AMENDMENTS TO THE CLAIMS

Sub C7

1. (Currently Amended): A method for manufacturing a semiconductor device comprising:

forming a dummy gate electrode on a semiconductor substrate having a predetermined length coincident with a length of a gate electrode to be formed;

with the dummy gate electrode used as a mask, forming one pair of first impurity diffusion layers in regions of the semiconductor substrate which are opposite to each other on opposite sides of the dummy gate electrode;

forming an insulating film on the semiconductor substrate so as to burry the dummy gate electrode and exposing an upper surface of the dummy gate electrode;

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removing the dummy gate electrode to form a first trench electrode in the insulating film having a width corresponding to at least the predetermined length of the dummy gate;

enlarging the width of the first trench on each side of the first trench by a predetermined amount to form a second trench in the insulating film <u>without etching the semiconductor substrate</u>, said predetermined amount being equal to or greater than a thickness of a gate insulation film to be lined on an inner surface of the second trench;

lining the gate insulating film of said thickness along the inner surface of the second trench; and

forming the gate electrode in the second trench with only the gate insulating film intervening therebetween.

2. (Previously Amended): The method according to claim 1, further comprising:

after forming the first impurity diffusion layers, forming a side wall insulating film on a side wall surface of the dummy gate electrode; and

with the dummy gate electrode and the sidewall insulating film used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

3. (Previously Amended): The method according to claim 1, wherein the forming of a second trench includes performing an isotropic etching on the insulating film having the first trench formed therein.

Claim 4. (Canceled).

5. (Previously Amended): The method according to claim 1, wherein the forming of the gate insulating film includes using an insulating material having a relative dielectric constant of above 5.

6. (Previously Amended): The method according to claim 1, wherein the forming of a gate insulating film includes using an insulating material selected from the group consisting of Ta2O5, silicon nitride, Al2O3, BaSrTiO3, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

7. (Currently Amended): A method of manufacturing a semiconductor device, comprising:

forming a first insulating film on a semiconductor substrate;

sequentially forming a first semiconductor film and a second insulating film on the first insulating film;

forming a resist pattern on the second insulating film;

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with the resist pattern used as a mask, patterning the first semiconductor film and the second insulating film by an anisotropic etching to provide a stacked layer structure of the first semiconductor film and the second insulating film on the semiconductor substrate having a predetermined width coincident with a length of a gate electrode to be formed;

with the stacked layer structure used as a mask, ion-implanting an impurity in the semiconductor substrate to provide first impurity diffusion layers for a source and a drain;

forming a third insulating film over the semiconductor structure to bury the stacked layer structure;

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etching back the third insulating film to expose an upper surface of the stacked layer structure;

with the third insulating film used as a mask, removing the stacked layer structure to form a trench in the third insulating film;

after forming the trench, enlarging the width of the trench by an isotropic etching by a predetermined width amount on each side of the trench that is equal to or larger than a thickness of a fourth insulating film along an inner surface of the trench <u>without etching the semiconductor substrate</u>;

after enlarging the width of the trench, depositing the fourth insulating film of said thickness along the inner surface of the trench; and

forming a conductive layer on and in contact with the fourth insulating film to form said gate electrode of a length coincident with the predetermined width.

8. (Previously Amended): The method according to claim 7, further comprising:

after providing the first impurity diffusion layers, forming a sidewall insulating film on a sidewall of the stacked layer structure; and

with the sidewall insulating film and the staked layer structure used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

9. (Previously Amended): The method according to claim 7, wherein the enlarging of the width of the trench includes using, as the isotropic etching, an etching treatment including HF or NH4F.

10. (Previously Amended): The method according to claim 7, wherein the depositing of the fourth insulating film includes depositing by a chemical vapor deposition method or a sputtering method.

Claim 11. (Canceled).

12. (Previously Amended): The method according to claim 7, wherein the depositing of the fourth insulating film includes using an insulating material having a dielectric constant of above 5.

13. (Previously Amended): The method according to claim 7, wherein the depositing of the fourth insulating film includes using an insulating material selected from the group consisting of Ta2O5, silicon nitride, Al2O3, BaSrTiO3, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

Claims 14-18 (Withdrawn).